

The block diagram illustrates the architecture of a digital camera system, showing the flow of data and power between various components. The system is organized into several main functional blocks:

- 62 BODY:** The main housing of the camera, which houses the **IMAGER BOARD** and the **INTERFACE**.
- 66 IMAGER BOARD:** Contains the **CCD DRIVER**, **CCD** sensor, **ANALOG** circuitry, **A/D** converter, **TIMING** control, and a **POWER SUPPLY**.
- 64 INTERFACE:** Connects the camera body to a **POWER PC** and manages data flow between the **POWER PC**, **BUFFERS**, **PROM**, and **DRAM**.
- 70 POWER PC:** The central processing unit, which includes **BUFFERS**, **PROM**, and **DRAM** for data storage and processing.
- 72 PCMCIA SLOT:** Two slots for PCMCIA memory cards, connected to the **POWER PC**.
- 68 PROCESSING BOARD:** Contains the **JPEG COMPRESSION**, **COLOR PROCESSING**, and **PIXEL PROCESSING** blocks, along with its own **POWER SUPPLY**.
- DISPLAY BOARD:** Manages the output to the **COLOR LCD** and **STATUS LCD**, including **LCD DRIVER** and **SWITCH INTERFACE** components.
- 20 COLOR LCD:** The main display for the captured image.
- STATUS LCD:** A smaller display for status information.
- BATTERY:** Provides power to the **POWER PC** and the **IMAGER BOARD**.
- Inputs:** The system includes a **QCD** (Quick Control Dial), a **MIC** (Microphone), and **BUTTONS** for user interaction.

The diagram shows the interconnections between these components, including data paths (solid lines) and power paths (dashed lines).

FIG. 2

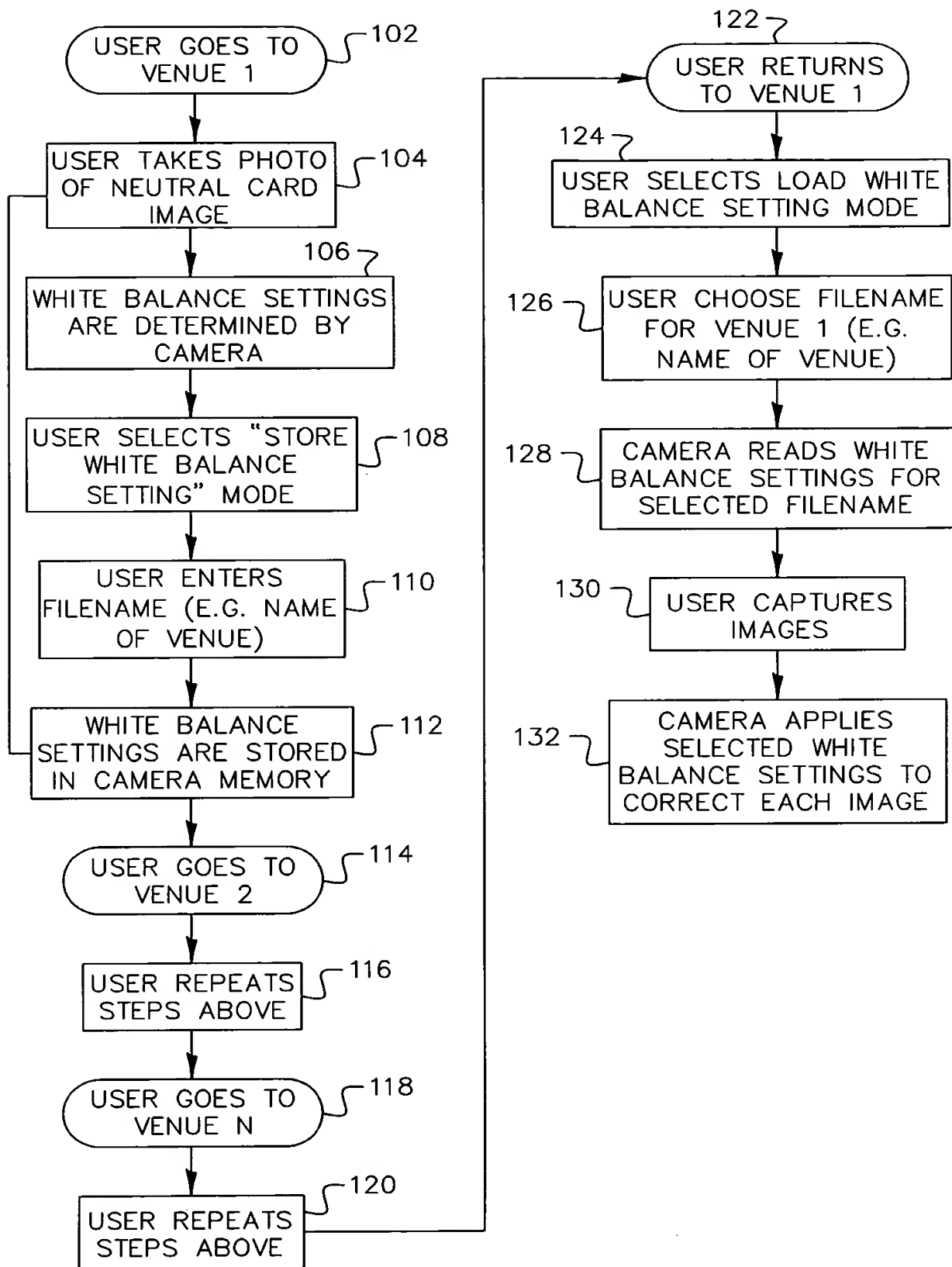


FIG. 3

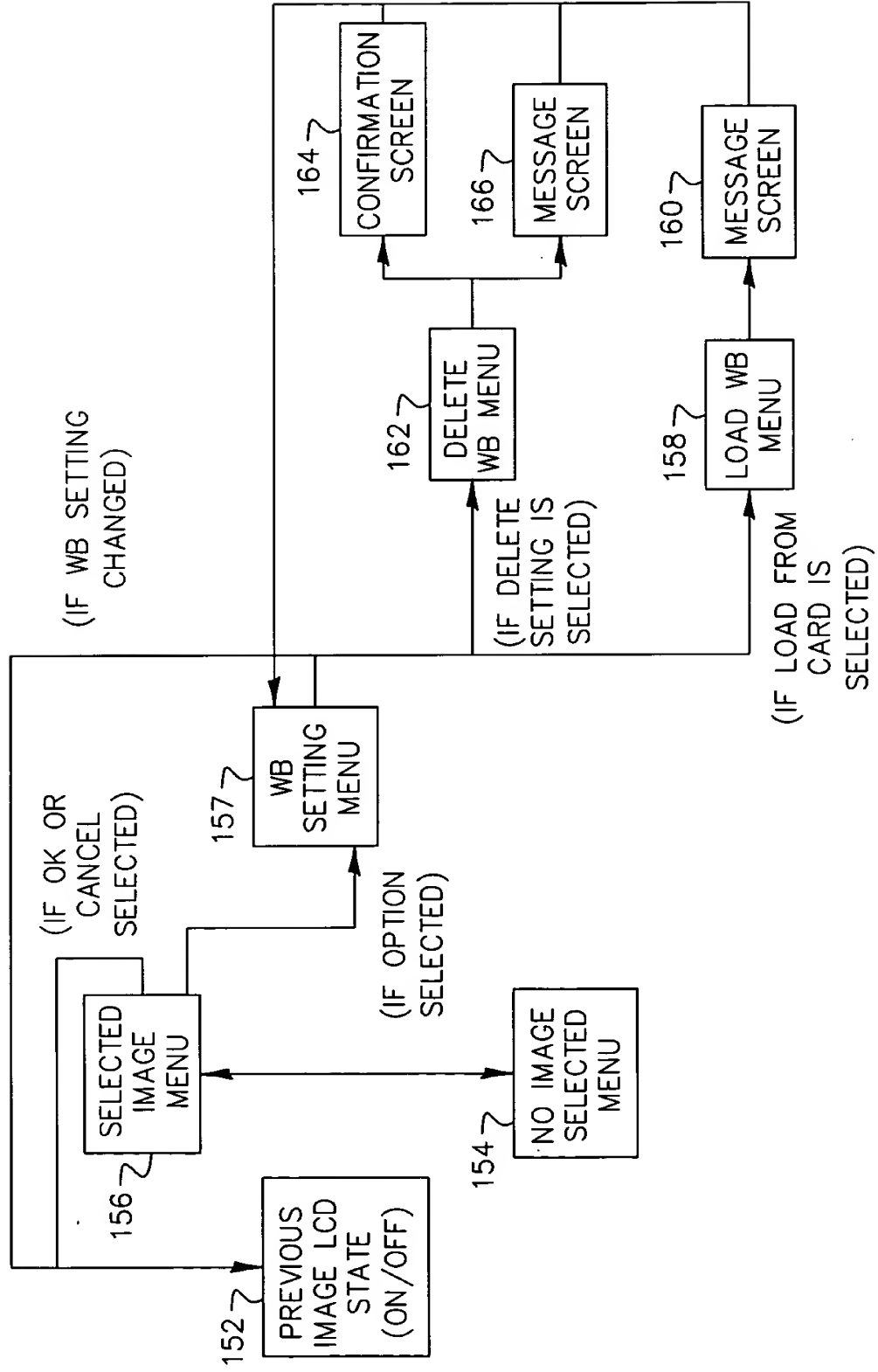


FIG. 4

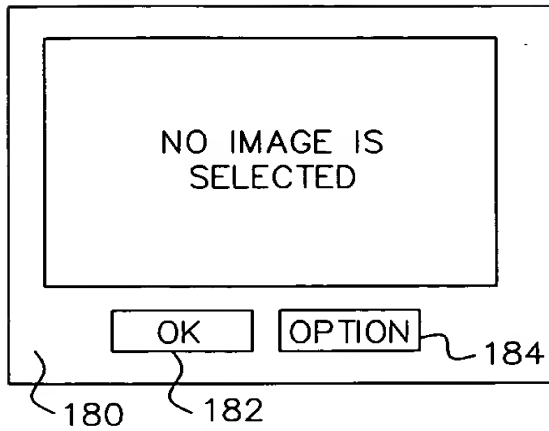


FIG. 5A

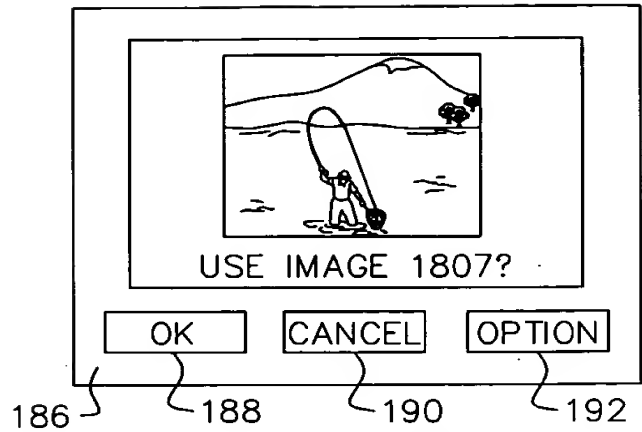


FIG. 5B

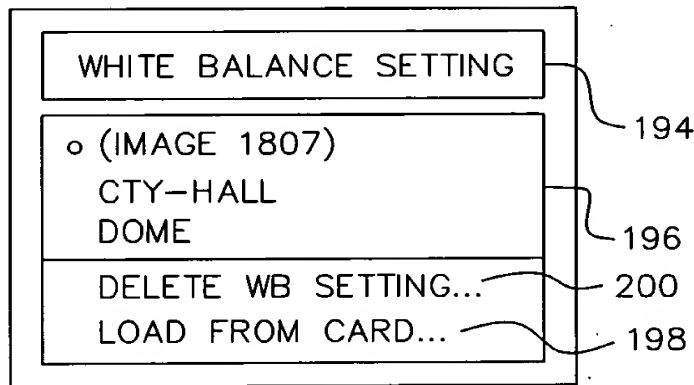


FIG. 5C

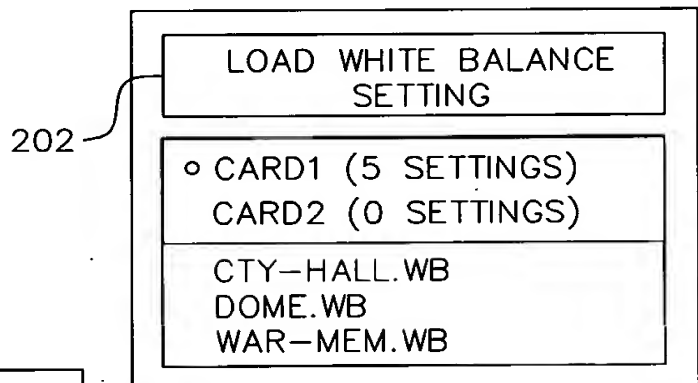


FIG. 5D

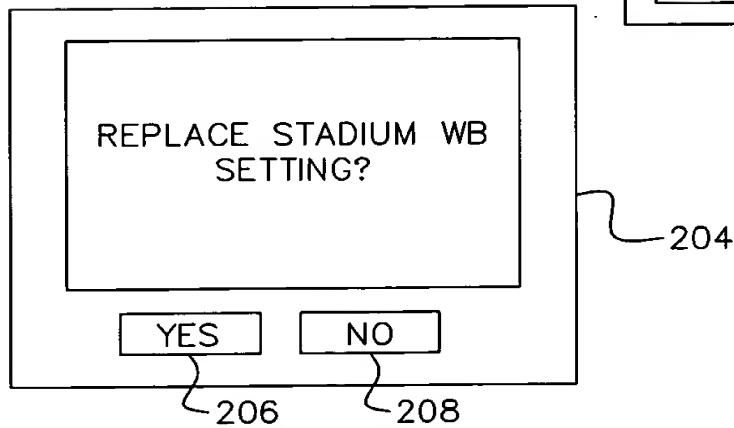


FIG. 5E

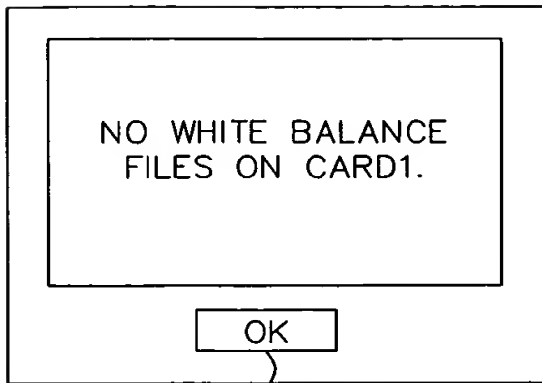


FIG. 5F

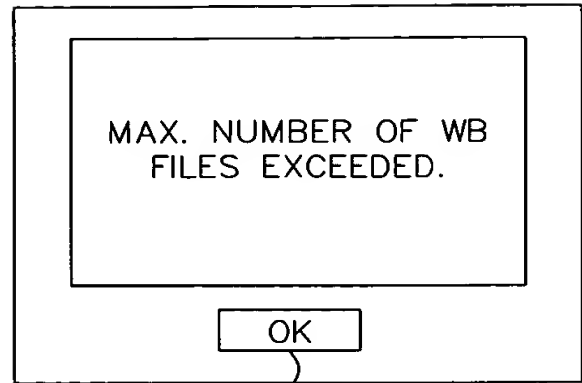


FIG. 5G

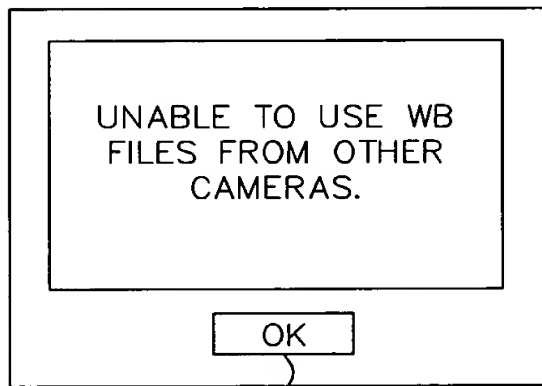


FIG. 5H

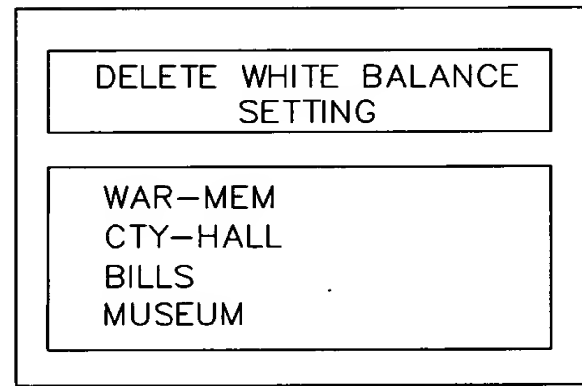


FIG. 5I

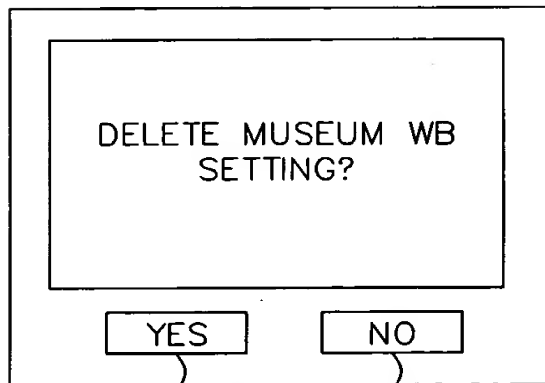


FIG. 5J

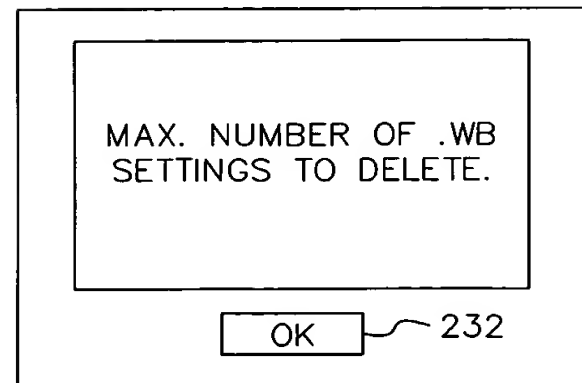


FIG. 5K